2-channel Gate Driver w/ LDO

■FEATURES

- ●Output Peak Current ±1A (peak)
- ●Operating Voltage Range 4V to 20V
- ●Fast Switching
  tr/tf=15ns/15ns(typ.) at CL=1,000pF
- ●Corresponding with Logic Voltage Operation: 3V/5V
- ●LDO Output Capability 5V / 50mA
- ●Thermal Shutdown
- ●Under Voltage Lockout (UVLO)
- ●Package Outline HSOP8, DFN8-V1

■GENERAL DESCRIPTION

The NJW4860 is 2 channels Gate driver that peak current is 1A.

Also NJW4860 is integrated 5V/50mA LDO.

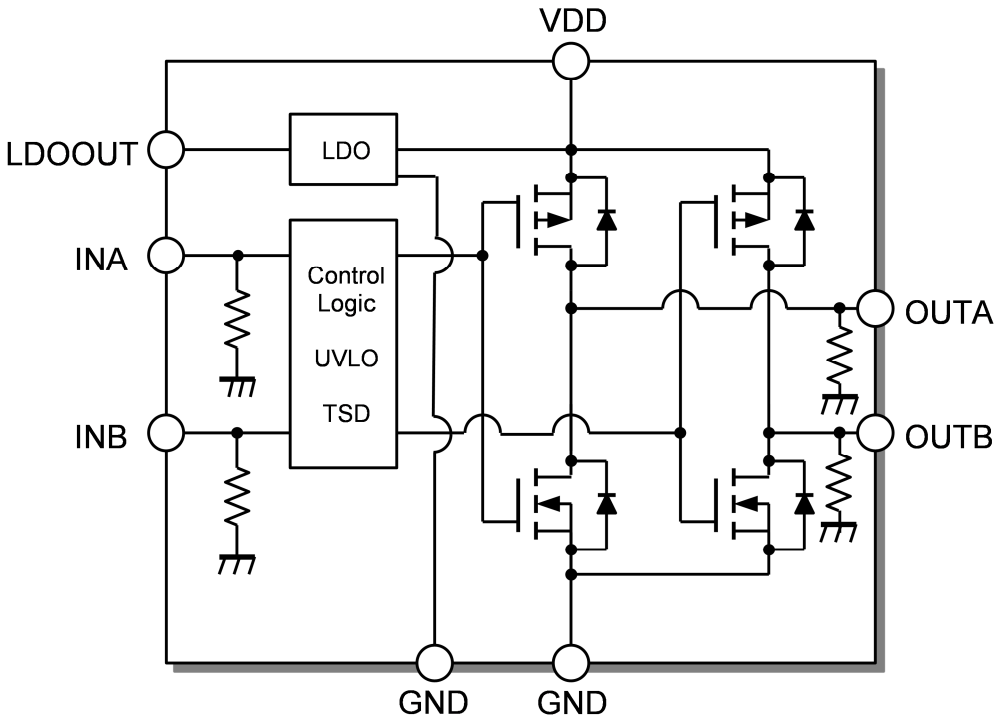
The NJW4860 other features are Withstand voltage of 45V, recommended operating voltage range: 4V to 20V and Fast switching time.

The NJW4860 is suitable for digital control applications.

■APPLICATION

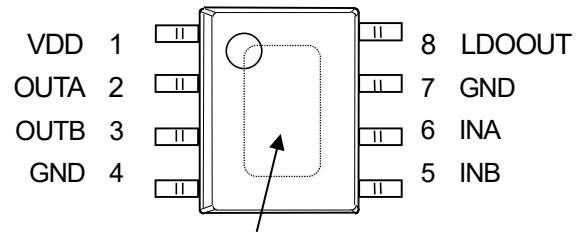
- ●Industrial Equipment
- ●LED Lighting
- ●Other

■BLOCK DIAGRAM

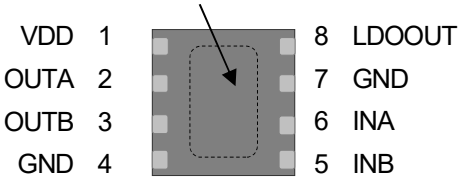


■PIN CONFIGURATION

[HSOP8]

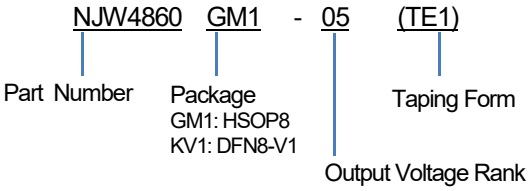


[DFN8-V1]



PIN NO.	SYMBOL	FUNCTION
1	VDD	Power Supply pin
2	OUTA	A channel Gate Driver Output pin
3	OUTB	B channel Gate Driver Output pin
4	GND	GND pin
5	INB	B channel Gate Driver Input pin
6	INA	A channel Gate Driver Input pin
7	GND	GND pin
8	LDOOUT	LDO Output pin

■PRODUCT NAME INFORMATION



■ORDERING INFORMATION

PART NUMBER	OUTPUT VOLTAGE RANK	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
NJW4860GM1-05(TE1)	5.0V	HSOP8	yes	yes	Sn100%	486050	81	3,000
NJW4860KV1-05(TE3)	5.0V	DFN8-V1	yes	yes	Sn2Bi	486050	7.2	3,000

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL		MAXIMUM RATINGS	UNIT	REMARK
Supply Voltage	V_{DD}		+45	V	VDD-GND pin
Input Voltage	V_{IN}		–0.3 to +6	V	INA/B-GND pin
Power Dissipation(Ta=25°C)	P_D	HSOP8	790 (1) 2,500 (2)	mW	–
		DFN8-V1	600 (3) 1,800 (4)		
Junction Temperature Range	Tj		–40 to +150	°C	–
Operating Voltage Range	T_{opr}		–40 to +125	°C	–
Storage Temperature Range	T_{stg}		–50 to +150	°C	–

(1): Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard, 2Layers)
(2): Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard, 4Layers),
internal Cu area: 74.2×74.2mm
(3): Mounted on glass epoxy board. (101.5 114.5 1.6mm: based on EIA/JEDEC standard, 2Layers FR-4,
with Exposed Pad)
(4): Mounted on glass epoxy board. (101.5 114.5 1.6mm: based on EIA/JEDEC standard, 4Layers FR-4,
with Exposed Pad)
(For 4Layers: Applying 99.5 99.5mm inner Cu area and thermal via holes to a board based
on JEDEC standard JESD51-5)

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT	REMARK
Supply Voltage (*5)	V_{DD}	4 to 20	V	VDD-GND pin
Input Voltage	V_{IN}	0 to 5.5	V	INA/B-GND pin

(5): When LDO is used, the minimum recommended operating voltage is 6V.
Also, it should be pay attention to the input voltage value so as not to exceed the package power dissipation.

■**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted, V_{DD}=15V、C_{IN}=1μF、C_O=1μF、Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
General						
Quiescent Current	I_{Q1}	V_{IN}=5V	–	2.5	4.0	mA
	I_{Q2}	V_{IN}=0V	–	2.1	3.6	mA
Gate Driver Output Block						
Output Peak Current	I_{PK1}	Pulse Width ≤10μs, V_{OUT}=0V	–	1	–	A
	I_{PK2}	Pulse Width ≤10μs, V_{OUT}=15V	–	1	–	A
Output ON Resistance	R_{DSH}	$I_{O\text{-}SOURCE}$=100mA	–	4.0	7.0	Ω
	R_{DSL}	$I_{O\text{-}SINK}$=100mA	–	3.3	6.0	Ω
Output Pulldown Resistance	R_{OUTPD}		60	100	140	kΩ
Gate Driver Input Block						
IN pin High Voltage	V_{IHIN}		2.0	–	5.5	V
IN pin Low Voltage	V_{ILIN}		0	–	0.8	V
Input Pulldown Resistance	R_{INPD}		60	100	140	kΩ
UVLO Block						
UVLO Release Voltage	V_{UVLO2}		2.8	3.3	3.8	V
UVLO Operating Voltage	V_{UVLO1}		2.5	3.0	3.5	V
UVLO Hysteresis Voltage	ΔV_{UVLO}	$V_{UVLO2} - V_{UVLO1}$	–	0.3	–	V
Output Rise/Fall characteristics						
Output Rise Time	tr	C_L=1,000pF, V_{IN}=0 to 5V	–	15	–	ns
Output Fall Time	tf	C_L=1,000pF, V_{IN}=5 to 0V	–	15	–	ns
Rise Delay Time	t_{d_ON}	C_L=1,000pF, V_{IN}=0 to 5V	–	40	–	ns
Fall Delay Time	t_{d_OFF}	C_L=1,000pF, V_{IN}=5 to 0V	–	45	–	ns
LDO Block						
Output Voltage	V_O	I_O=10mA	-1.0%	–	+1.0%	V
Output Current	I_O		0	–	50	mA
Line Regulation	$\Delta V_O/\Delta V_{DD}$	V_{DD} =6V to 20V, I_O=10mA	–	–	0.03	%/V
Load Regulation	$\Delta V_O/\Delta I_O$	I_O=0mA to 50mA	–	–	0.01	%/mA
Ripple Rejection	RR	V_{DD} = 6V ,ein=200mVrms, f=1kHz, I_O =10mA	–	60	–	dB
Dropout Voltage	ΔV_{DD}	I_O=10mA	–	0.03	0.1	V
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta Ta$	Ta=-40°C to +125°C, I_O=10mA	–	±50	–	ppm/°C

■THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE		UNIT
Junction-to-ambient thermal resistance	θja	HSOP8	158 (6) 50 (7)	°C /W
		DFN8-V1	208 (8) 68 (9)	
Junction-to-ambient thermal resistance	ψjt	HSOP8	28 (6) 12 (7)	°C /W
		DFN8-V1	15 (8) 7 (9)	

(1): Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard, 2Layers)
(2): Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard, 4Layers), internal Cu area: 74.2×74.2mm
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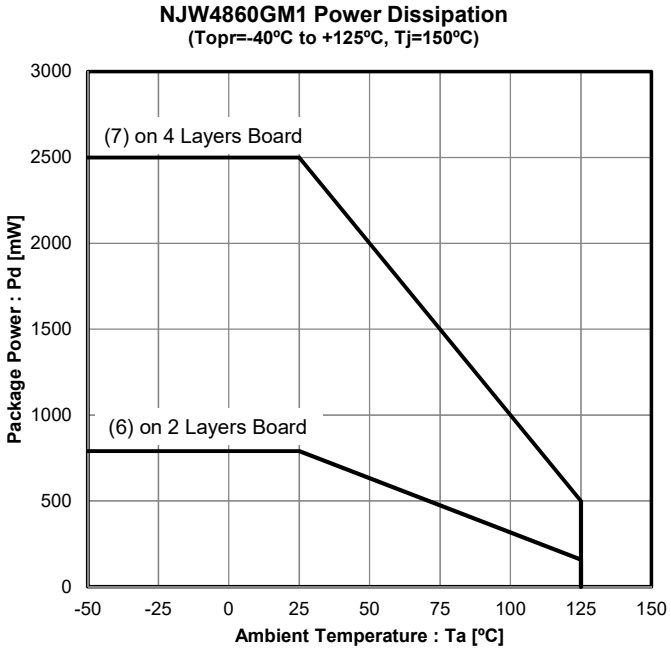
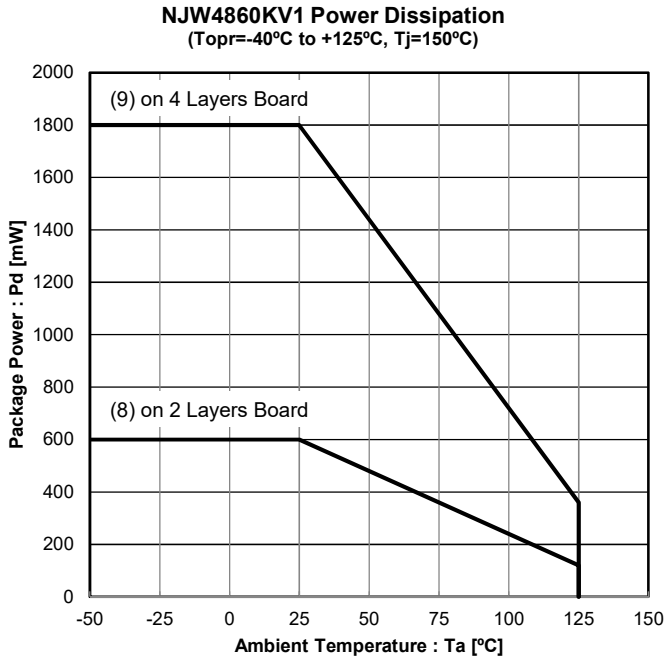
(For 4Layers: Applying 99.5 99.5mm inner Cu area and thermal via holes to a board based on JEDEC standard JESD51-5)

■POWER DISSIPATION vs. AMBIENT TEMPERATURE





■TIMING CHART

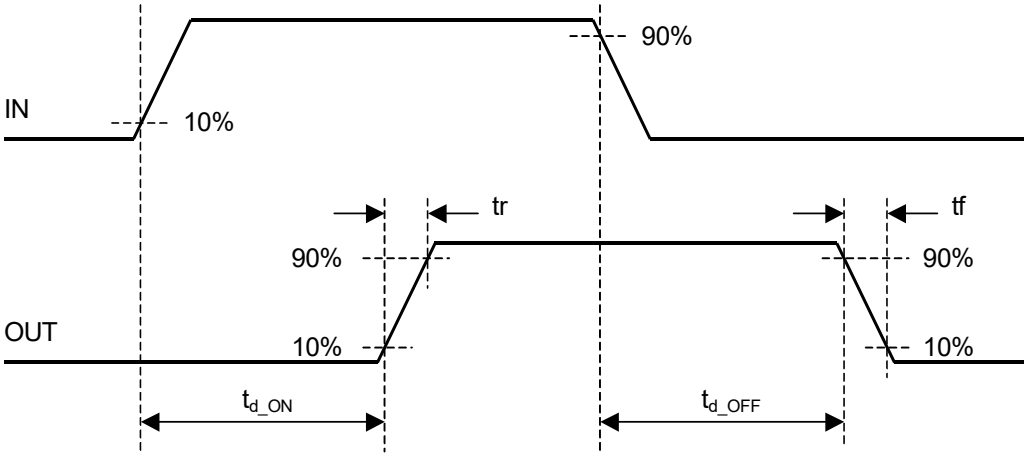
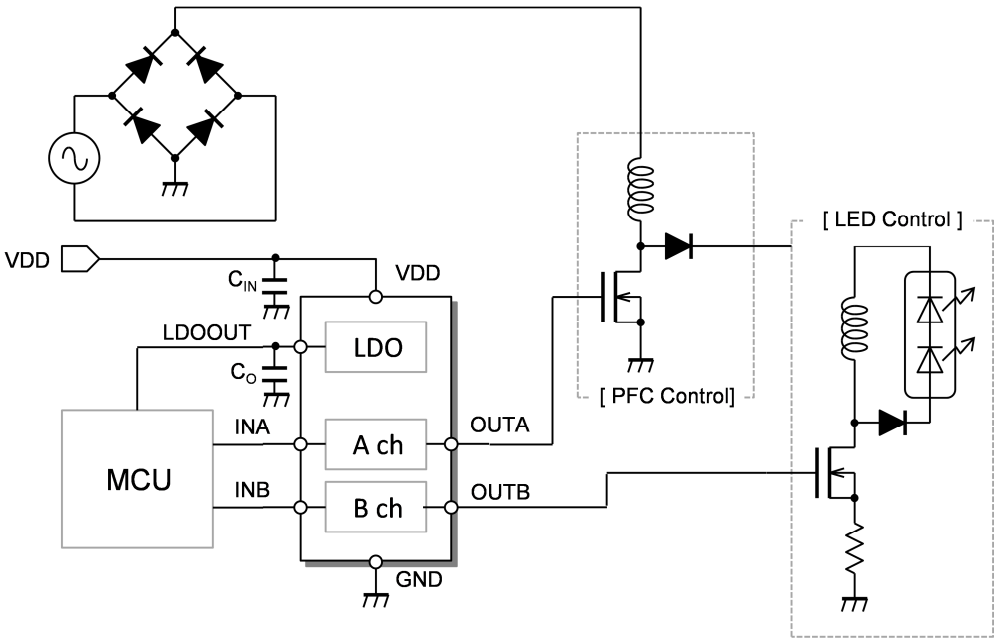


Fig1. Output Rise/Fall Time, Rise/Fall Delay Time

■TYPICAL APPLICATION



In the application that does a high-speed switching of NJW4860, because the current flow corresponds to the output rise and fall, the substrate (PCB) layout becomes an important. NJW4860 is driving the MOSFET with high speed to reduce switching losses. The transient voltage is generated by parasitic inductance and a high-speed current change of MOSFET. It should be attempt the transition voltage decrease by making a current loop area minimize as much as possible. Therefore, it should make a current flowing line thick and short as much as possible. It should insert a bypass capacitor between VDD pin and GND pin to prevent malfunction by generating over voltage and/or exceed maximum input voltage rating. The recommended bypass capacitor is low ESR and high frequency characteristic (NJRC recommends 1μF or more). An aluminum electrolysis capacitor is recommended for smoothing condenser. (NJRC recommends 10μF or more). However, you should use large capacitor by sufficient evaluation (assessment) due to load condition and/or application use environment. The bypass capacitors should be connected as much as possible near VDD pin.

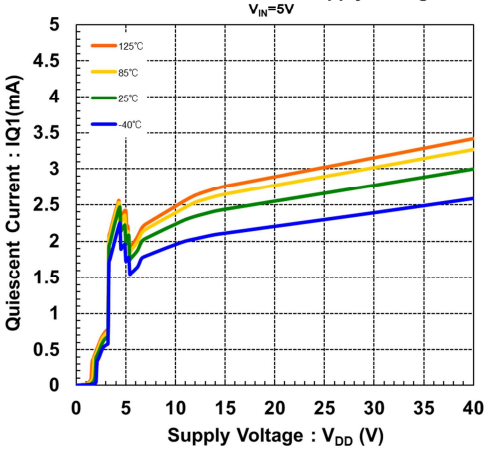
Also, the output capacitor C_O is required for a phase compensation of the internal LDO's error amplifier, and the capacitance and the equivalent series resistance (ESR) influence stable operation of the regulator. If use a smaller output capacitor than the recommended capacitance (refer to conditions of ELECTRIC CHARACTERISTIC), it may cause excess output noise or oscillation of the regulator due to lack of the phase compensation. Therefore, the recommended capacitance or larger output capacitor, connected between LDOOUT and GND as short path as possible, is recommended for stable operation.

Furthermore, a larger output capacitor reduces output noise and ripple output, and also improves Output Transient Response when a load changes rapidly.

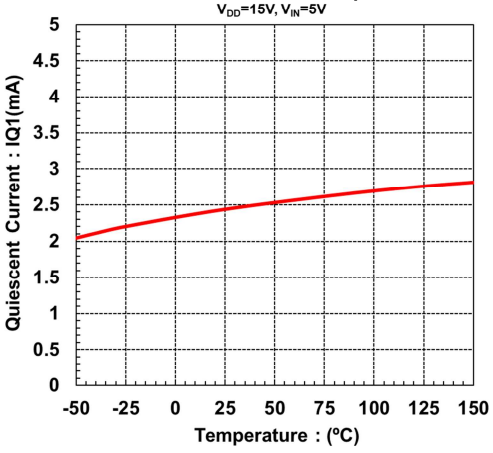
Selecting the output capacitor, should consider varied characteristics of a capacitor: frequency characteristics, temperature characteristics, DC bias characteristics and so on. Therefore, the capacitor that has a sufficient margin of the rated voltage against the output voltage and superior temperature characteristics is recommended for C_O.

■TYPICAL CHARACTERISTICS

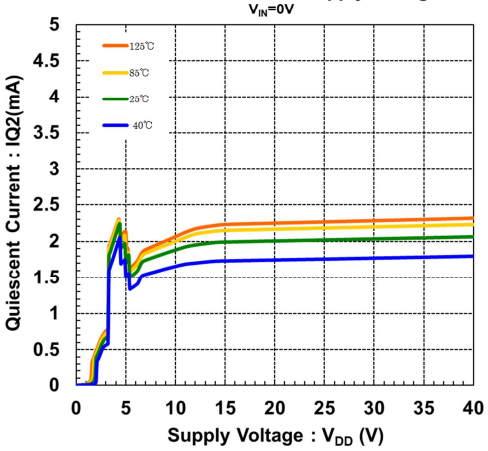
Quiescent Current vs Supply Voltage
V_{IN}=5V



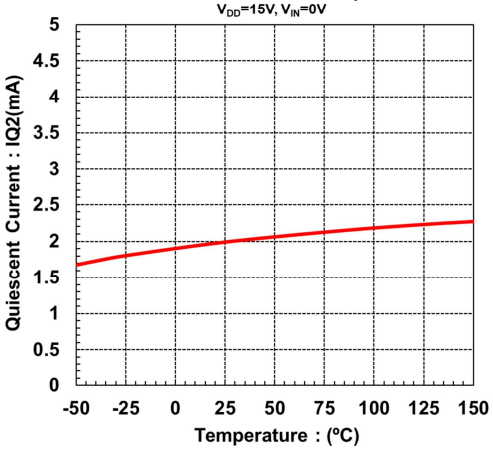
Quiescent Current vs Temperature
V_{DD}=15V, V_{IN}=5V



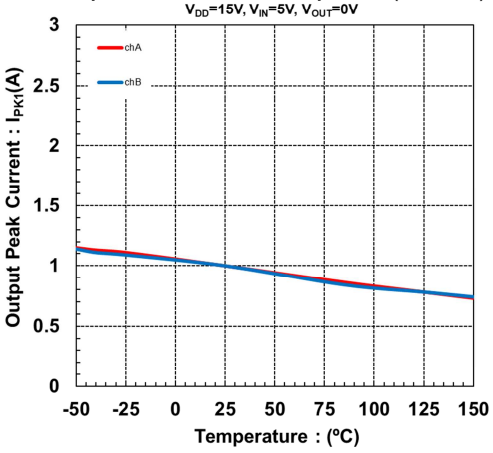
Quiescent Current vs Supply Voltage
V_{IN}=0V



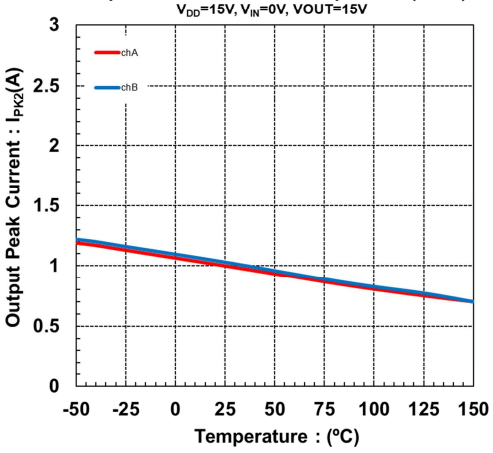
Quiescent Current vs Temperature
V_{DD}=15V, V_{IN}=0V



Output Peak Current vs Temperature(SOURCE)
V_{DD}=15V, V_{IN}=5V, V_{OUT}=0V

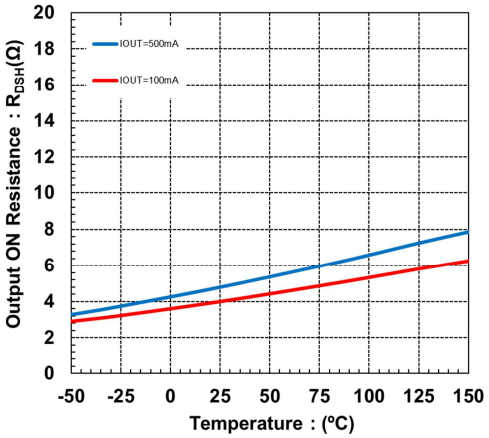


Output Peak Current vs Temperature(SINK)
V_{DD}=15V, V_{IN}=0V, VOUT=15V

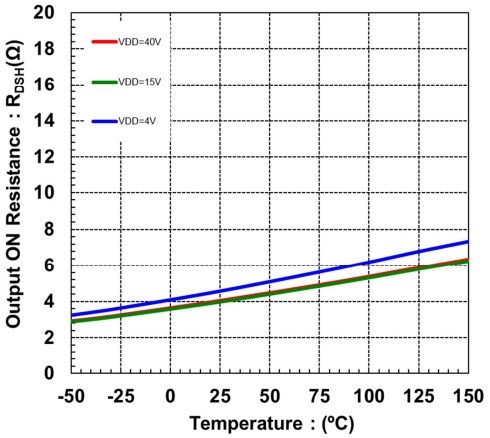


■TYPICAL CHARACTERISTICS

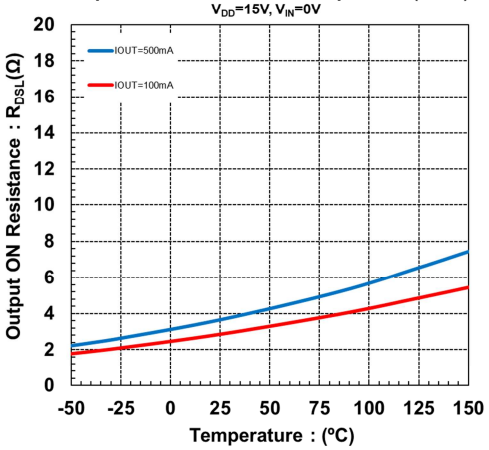
Output ON Resistance vs Temperature(SOURCE)
V_{DD}=15V, V_{IN}=5V



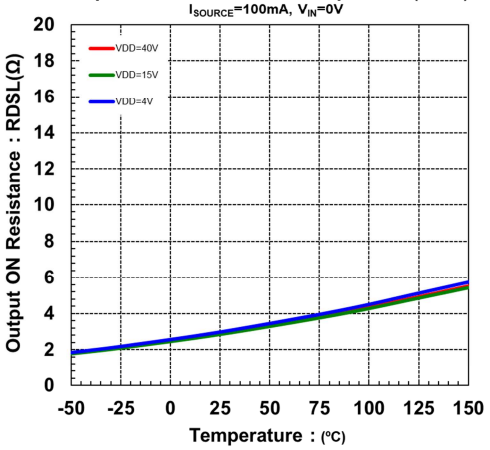
Output ON Resistance vs Temperature(SOURCE)
I_{SOURCE}=100mA, V_{IN}=5V



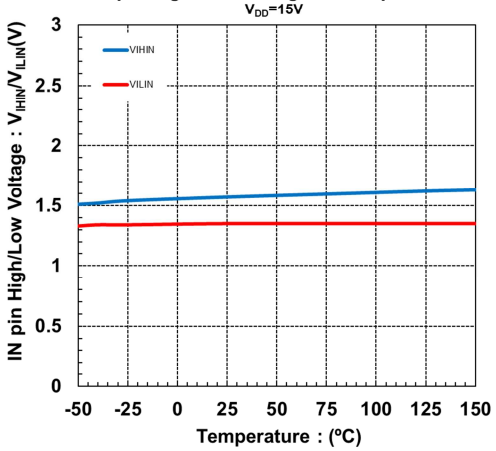
Output ON Resistance vs Temperature(SINK)
V_{DD}=15V, V_{IN}=0V



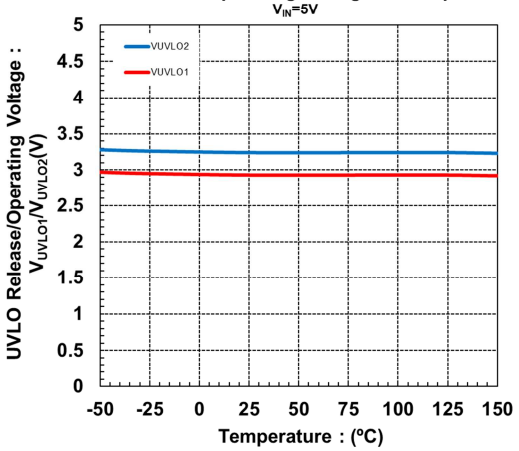
Output ON Resistance vs Temperature(SINK)
I_{SOURCE}=100mA, V_{IN}=0V



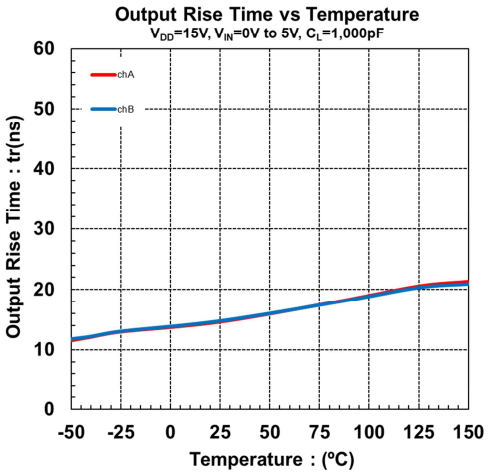
IN pin High/Low Voltage vs Temperature
V_{DD}=15V

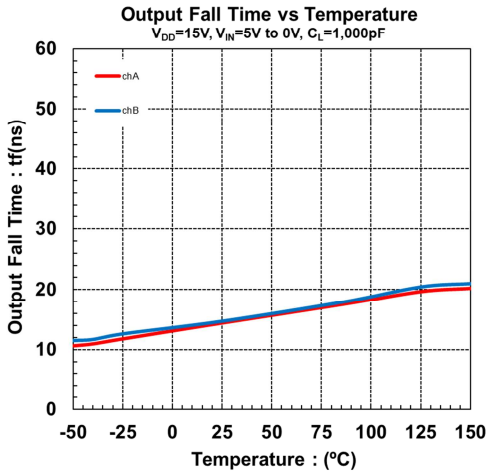


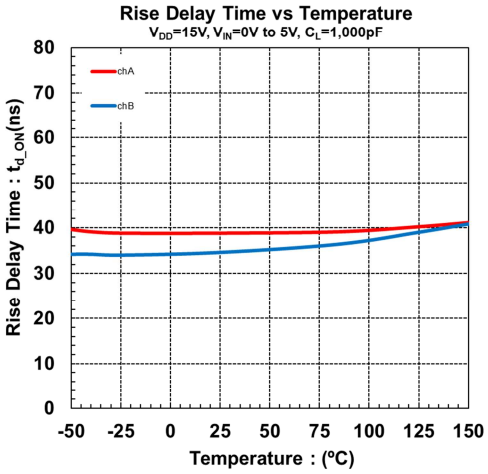
UVLO Release/Operating Voltage vs Temperature
V_{IN}=5V

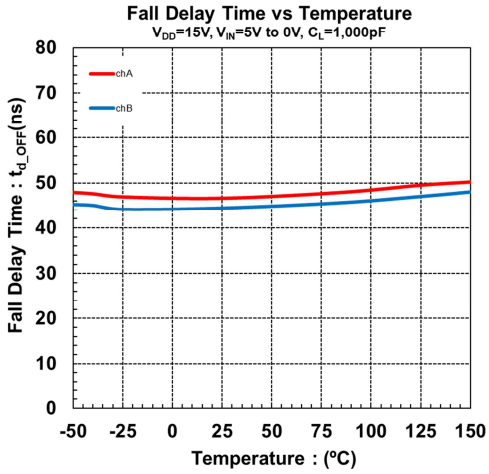


■TYPICAL CHARACTERISTICS

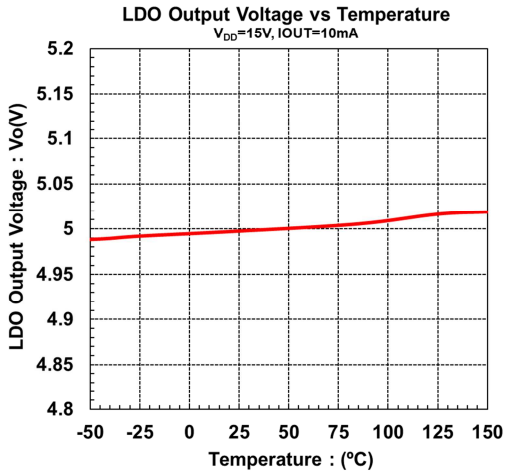


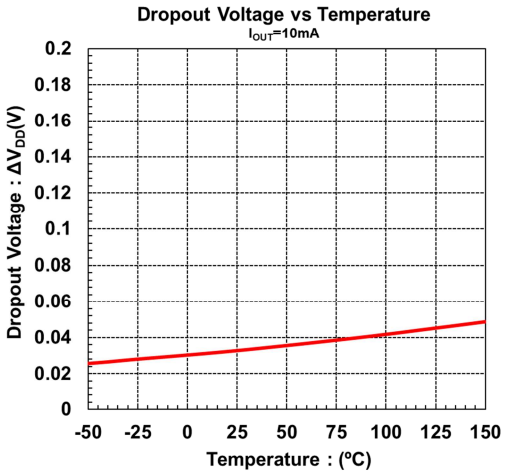


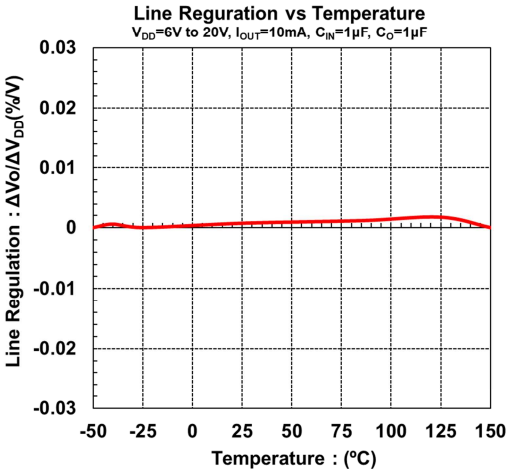


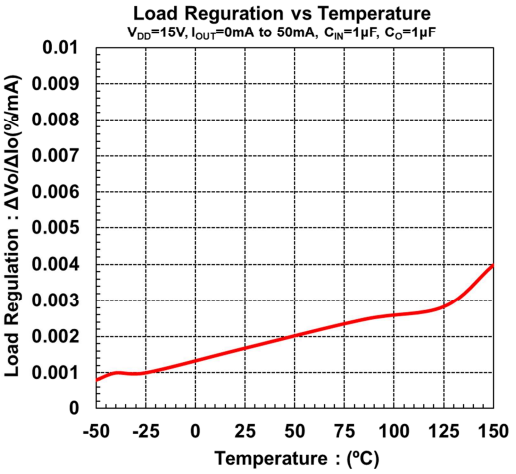


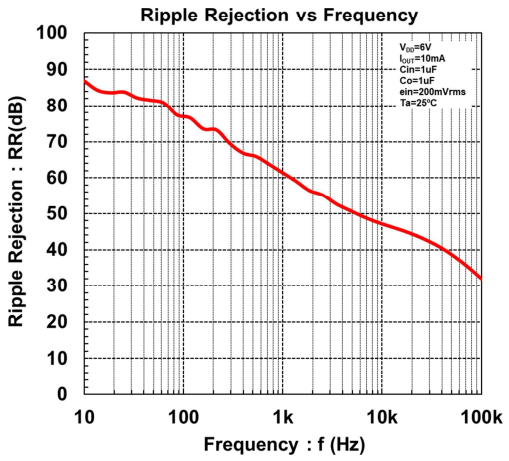
■TYPICAL CHARACTERISTICS

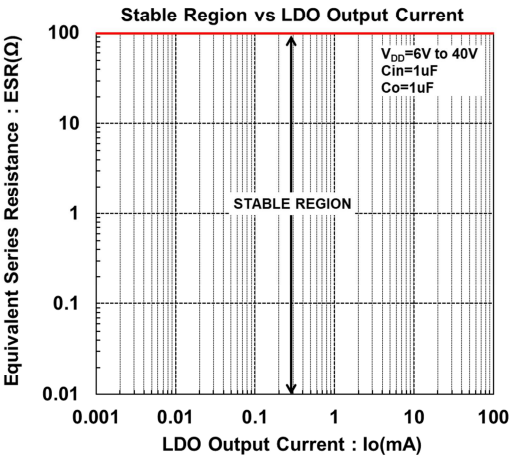








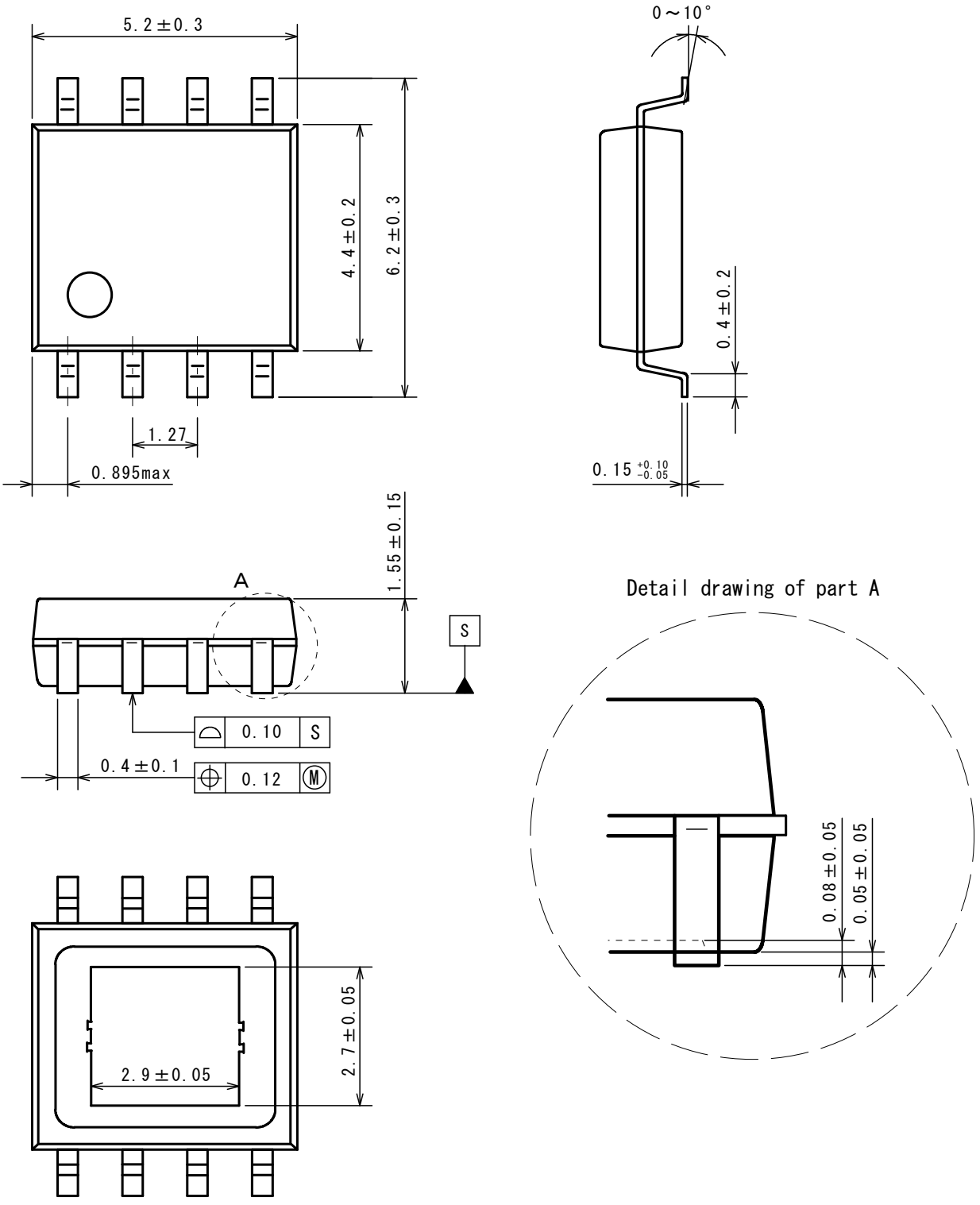




HSOP8

Unit: mm

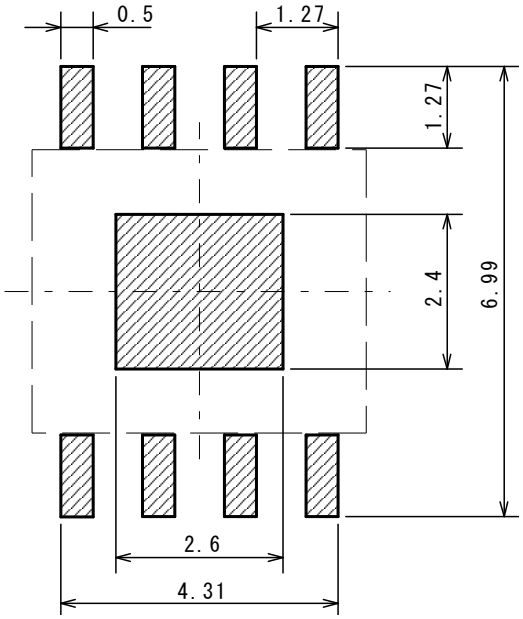
■PACKAGE DIMENSIONS



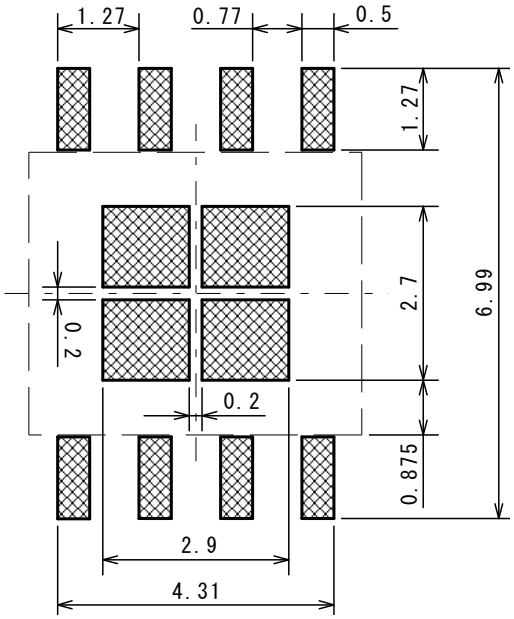
HSOP8

Unit: mm

■EXAMPLE OF SOLDER PADS DIMENSIONS



<Solder pattern>



<Metal mask>

<Instructions for mounting>

Please note the following points when you mount HSOP-8 package IC because there is a standoff on the backside electrode.

(1) Temperature profile of lead and backside electrode.

It is necessary that both re-flow temperature profile of lead and backside electrode are higher than preset temperature.

When solder wet temperature is lower than lead/backside electrode temperature, there is possibility of defect mounting.

(2) Design of foot pattern / metal mask

Metal mask thickness of solder pattern print is more than 0.13mm.

(3) Solder paste

The mounting was evaluated with following solder paste, foot pattern and metal mask.

Because mounting might be greatly different according to the manufacturer and the product number even if the solder composition is the same.

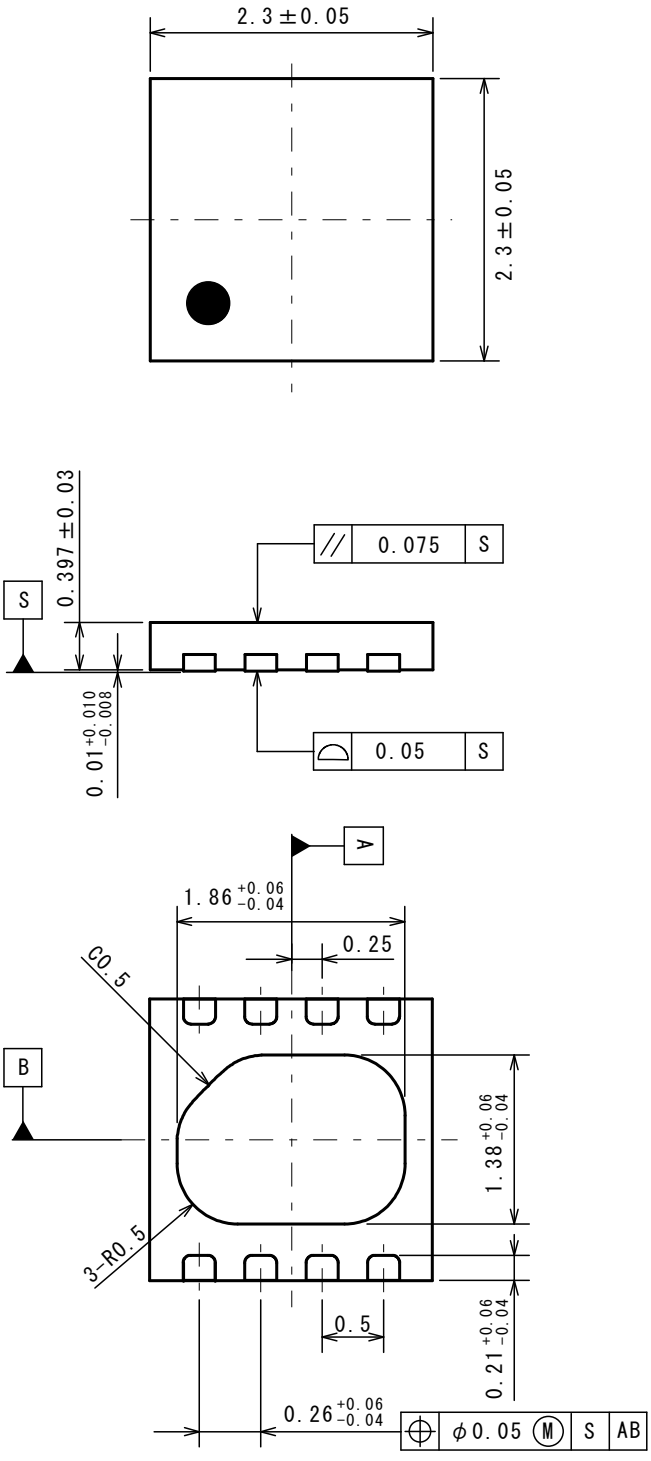
We will strongly recommend to evaluate mounting previously with using foot pattern, metal mask and solder paste.

Solder paste composition	Sn37Pb (Senju Metal Industry Co., Ltd : OZ7053-340F-C)
	Sn3Ag0.5Cu (Senju Metal Industry Co., Ltd : M705-GRN350-32-11)

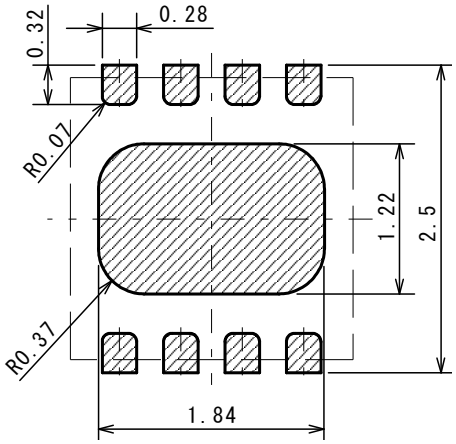
DFN8-V1

Unit: mm

■PACKAGE DIMENSIONS



■EXAMPLE OF SOLDER PADS DIMENSIONS

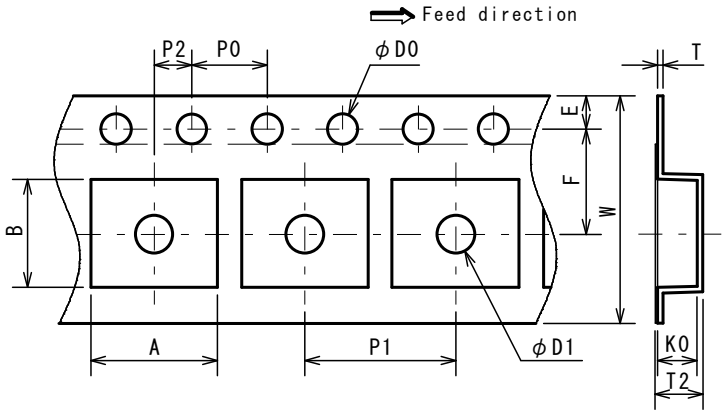


HSOP8

■PACKING SPEC

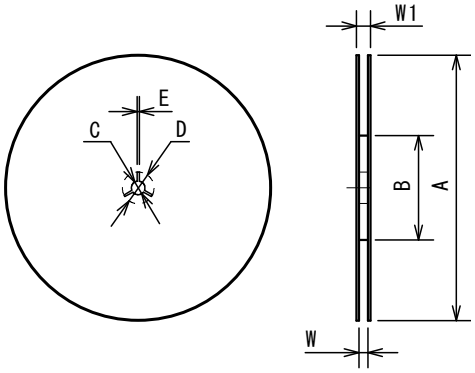
Unit: mm

TAPING DIMENSIONS



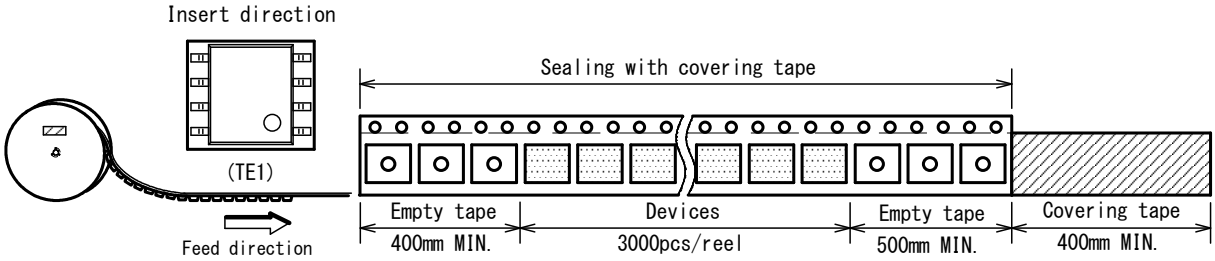
SYMBOL	DIMENSION	REMARKS
A	6.7±0.1	
B	5.55±0.1	
D0	1.55±0.05	
D1	2.05±0.05	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.3±0.05	
T2	2.47	
K0	2.1±0.1	
W	12.0±0.2	

REEL DIMENSIONS

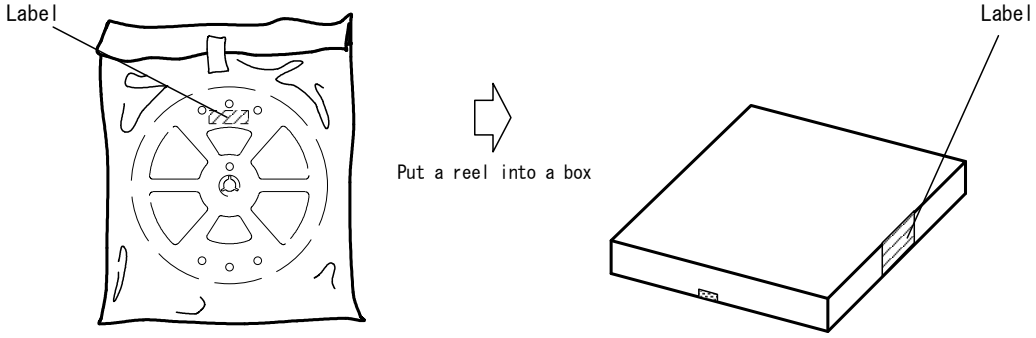


SYMBOL	DIMENSION
A	φ330±2
B	φ 80±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	13.5±0.5
W1	17.5±1

TAPING STATE



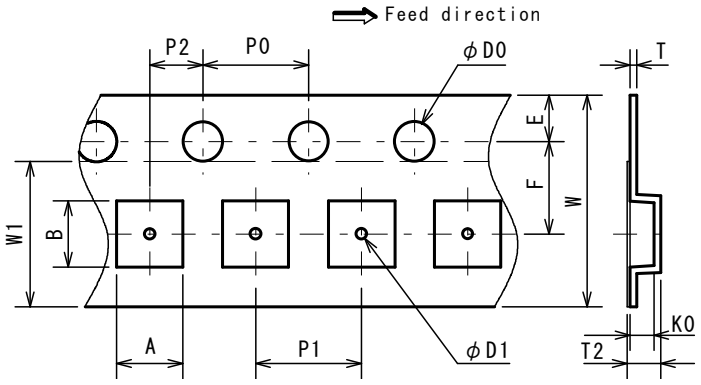
PACKING STATE



■PACKING SPEC

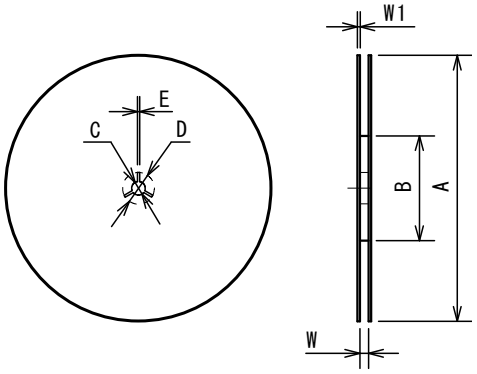
Unit: mm

TAPING DIMENSIONS



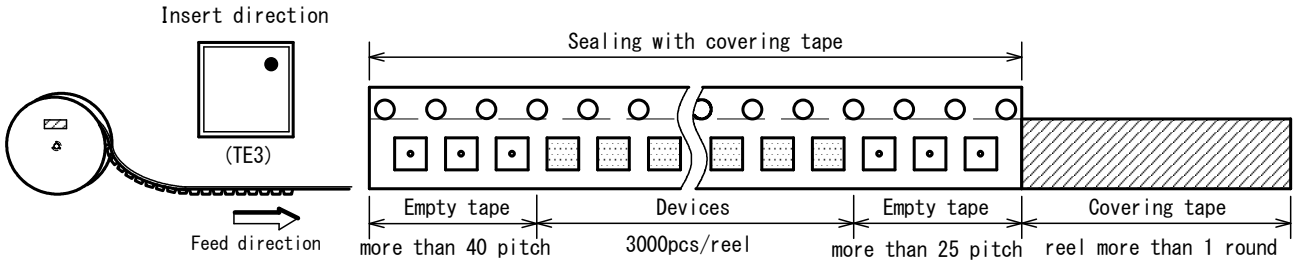
SYMBOL	DIMENSION	REMARKS
A	2.55±0.05	BOTTOM DIMENSION
B	2.55±0.05	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	0.5±0.1	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.00±0.07	
K0	0.65±0.05	
W	8.0±0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

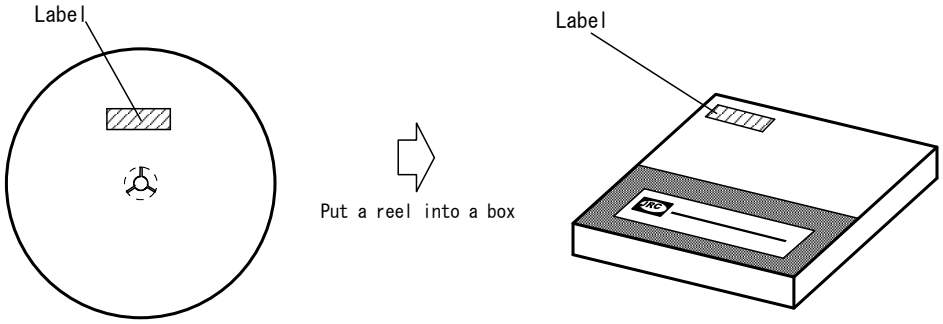


SYMBOL	DIMENSION
A	$\phi 180^{0}_{-1.5}$
B	ϕ 60 $^{+1}_{0}$
C	ϕ 13±0.2
D	ϕ 21±0.8
E	2±0.5
W	$9^{+0.3}_{0}$
W1	1.2

TAPING STATE



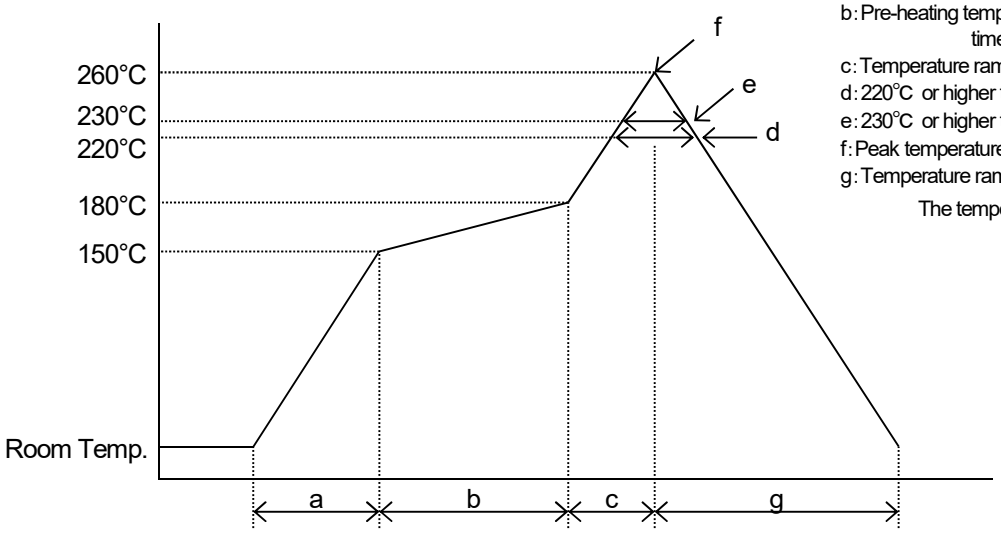
PACKING STATE



■RECOMMENDED MOUNTING METHOD

・INFRARED REFLOW SOLDERING METHOD

*Recommended reflow soldering procedure



a: Temperature ramping rate	: 1 to 4°C /s
b: Pre-heating temperature	: 150 to 180°C
time	: 60 to 120s
c: Temperature ramp rate	: 1 to 4°C /s
d: 220°C or higher time	: Shorter than 60s
e: 230°C or higher time	: Shorter than 40s
f: Peak temperature	: Lower than 260°C
g: Temperature ramping rate	: 1 to 6°C /s

The temperature indicates at the surface of mold package.

■REVISION HYSTORY

Date	Revision	Changes
15.Feb.2018	Ver.1	New Release
20.Jul.2018	Ver.1.1	Corrected of ABSOLUTE MAXIMUM RATINGS (Power Dissipation) and ORDERING INFORMATION (MARKING)

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