Features

- 2500-V_{RMS} Isolation
  - UL 1577 approved
- Integrated Transient Voltage Suppressor (TVS) for A and B of bus-side to guarantee
- IEC61000-4-2 8kV (Contact)
- HBM ±8kV ESD Protection for all pins
- MM ±600V ESD Protection for all pins
- CDM ±1kV ESD Protection for all pins
- Latchup immunity up to ±400mA
- Hot-Swap Glitch Protection on Control Inputs
- Up to 256 Transceivers on the Bus
- 3.3-V Inputs are 5-V Tolerant

Applications

- Energy Meter Networks
- Motor Control
- Industrial Control
- Telecommunications Equipment
- Factory Automation
- Security System

Description

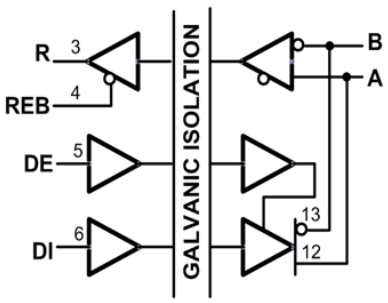
The AZRS6412 which includes one transmitter and one receiver is isolated half-duplex differential transceiver for TIA/EIA 485/422 applications. The galvanic isolation barrier of the device has tested to provide at least 2500 V_{RMS} of isolation for 60s between the interface of the bus-side and the logic-side.

The AZRS6412 features a true fail-safe receiver, which guarantees the output of receiver to logic high when the differential inputs (bus pins, A and B) of the receiver are open, short or idle.

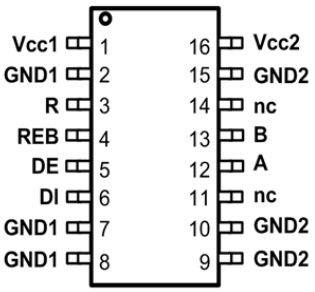
The AZRS6412 has the current limited circuits in the transmitter to protect the device from damage by the system fault conditions during normal operation.

The AZRS6412 features a hot-swap glitch-free design which guarantees outputs of the transmitter and the receiver in a high impedance state during the power up period. It is designed 1/8 unit load with minimum 96kΩ of input impedance, which can connect 256 devices on a bus at least. The high-reliable AZRS6412 with built-in system level ESD protection can against high-energy noise transients without requiring any external components.

Function Diagram



DW Package
Top View



Functional Block and Pin Configuration

Part Number	Duplex	Tx/Rx	Data Rate (Kbps)	Rx Input Filtering	Power On Reset	Tx/ Rx Enable	Package Type
AZRS6412	Half	1/1	200	Yes	Yes	Yes	WSOIC-16

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNITS
Power Supply Vcc	V_{CC1}, V_{CC2}	-0.3 to 6.0	V
Control Input Voltage	REB, DE	-0.3 to (Vcc+ 0.3)	V
Receiver Input Voltage	A, B	±13	V
Receiver Output Voltage	RO	-0.3 to (Vcc+ 0.3)	V
Transmitter Output Voltage	A, B	±13	V
Transmitter Input	DI	-0.3 to (Vcc+ 0.3)	V
Operating Temperature	T_{OP}	-40 to +85	°C
Storage Temperature	T_{STO}	-65 to +150	°C

PARAMETER	Standard	Pins	RATING	UNITS
ESD	IEC61000-4-2 Contact	A, B	8	kV
	Human Body Model (JEDEC standard 22)	All pins	8	kV
	Machine Model (ANSI/ESDS5.2-1996)	All pins	±600	V
	Charge Device Model	All pins	±1	kV
Latchup	EIA/JESD78	All pins	±400	mA

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic-side Supply Voltage	V_{CC1}	3.15		5.5	V
Bus-side Supply Voltage	V_{CC2}	4.5	5.0	5.5	V
Voltage at Bus Terminal (A, B)	V_{OC}	-7		12	V
High-level Input Voltage(DI, DE, REB)	V_{IH}	2		Vcc	V
Low-level Input Voltage(DI, DE, REB)	V_{IL}	0		0.8	V
Output Current of Driver	I_{OD}	-50		50	mA
Output Current of Receiver	I_{OR}	-2		2	mA
Termination Resistance	R_T	54	60		Ω
Operating Temperature	T_{OP}	-40		85	°C

DC ELECTRICAL CHARACTERISTICS

(3.15V≤V_{CC1}≤5.5V, 4.5V≤V_{CC2}≤5.5V with T_{AMB}= T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC1}=3.3V, V_{CC2}=5.0V and T_{AMB}= 25 °C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMITTER							
Differential Transmitter Output	V_{OD}	Fig.1, No load				V_{CC}	V
Differential Transmitter Output	V_{OD}	Fig.2, R_L= 27Ω		1.5			V
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	Fig.2 , R_L= 27Ω		-0.2		0.2	V
Transmitter Common- Mode Output Voltage	V_{OC}	Fig.2, R_L= 27Ω				3.1	V
Change in Magnitude of Common- Mode Voltage	ΔV_{OC}	Fig.2, R_L= 27Ω				0.2	V
Input High Voltage	V_{IH}	DE, DI		2.0			V
Input Low Voltage	V_{IL}	DE, DI				0.8	V
Input Current	I_{IND}	DE, DI=0V or V_{CC1}		-10		+10	μA
DI Input Hysteresis	V_{HYS}				100		mV
Transmitter Short-Circuit Output Current	I_{OS}	Fig.6, -7V ≤ VOUT ≤ 12V		-250		250	mA
RECEIVER							
Receiver Differential Threshold Voltage	V_{TH}			-200		-50	mV
Receiver Input Hysteresis	V_{hys}				20		mV
Receiver Output High Voltage	V_{OH}	Fig.7, Io= -2mA, VID= 200mV	V_{CC1}=3.3V	V_{CC1}-0.4	3.0		V
			V_{CC1}=5V	V_{CC1}-1	4.7		
Receiver Output Low Voltage	V_{OL}	Fig.7,Io= 2mA, VID= -200mV	V_{CC1}=3.3V		0.15	0.4	V
			V_{CC1}=5V		0.15	0.4	
Three- State Output Current	I_{OZR}	0V ≤ V_I ≤ V_{CC1}		-1		1	μA
Bus Input Current	I_{INR1}	V_A or V_B=12V, V_{CC2}=5V	Other input at 0V		0.08	0.1	mA
		V_A or V_B=12V, V_{CC2}=0V			0.1	0.13	
		V_A or V_B=-7V, V_{CC2}=5V		-0.1	-0.07		
		V_A or V_B=-7V, V_{CC2}=0V		-0.06	-0.05		
Input Current	I_{INR2}	REB =0V or V_{CC1}		-10		+10	μA
Input High Voltage	V_{IH}	REB		2.0			V
Input Low Voltage	V_{IL}	REB				0.8	V
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ +12V		96			kΩ

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Logic-side Supply Current (3.3V V_{CC1})	I_{CC1}	REB= 0 or V_{CC1}, DE= 0 or V_{CC1}.		2	3	mA
Logic-side Supply Current (5V V_{CC1})	I_{CC1}	REB= 0 or V_{CC1}, DE= 0 or V_{CC1}.		3	5	mA
Bus-side Supply Current	I_{CC2}	REB= 0 or V_{CC1}, DE= 0, No load.		4	8	mA

SWITCHING CHARACTERISTICS

(3.15V≤V_{CC1}≤5.5V, 4.5V≤V_{CC2}≤5.5V with T_{AMB}= T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC1}=3.3V, V_{CC2}=5.0V and T_{AMB}= 25 °C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter Input to Output	t_{DPLH}, t_{DPHL}	Fig.3,R_{DIFF}=54Ω, C_{L1}=C_{L2}= 100pF		2	3	us
Transmitter Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}			0.5	1	us
Transmitter Rise or Fall Time	t_{DF}, t_{DR}			150	400	ns
Maximum Data Rate	f_{MAX}				200	Kbps
Transmitter Enable to Output Low	t_{DZL}	Fig.5, C_{DL}=50pF			3	us
Transmitter Enable to Output High	t_{DZH}	Fig.4, C_{DL}=50pF			3	us
Transmitter Disable Time from Low	t_{DLZ}	Fig.5, C_{DL}=50pF			3	us
Transmitter Disable Time from High	t_{DHZ}	Fig.4, C_{DL}=50pF			3	us
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Fig.8, $\lvert V_{ID} \rvert \geq$ 2.0V; rise and fall time of $V_{ID} \leq$ 15ns		2	3	us
$\lvert t_{RPLH} - t_{RPHL} \rvert$ Different Receiver Skew	t_{RSKD}			0.5	1	us
Receiver Enable to Output Low	t_{RZL}	Fig.10, C_{RL}=15pF			3	us
Receiver Enable to Output High	t_{RZH}	Fig.9, C_{RL}=15pF			3	us
Receiver Disable Time from Low	t_{RLZ}	Fig.10, C_{RL}=15pF			3	us
Receiver Disable Time from High	t_{RHZ}	Fig.9, C_{RL}=15pF			3	us

PIN FUNCTION DESCRIPTION

Pin Number	Mnemonic	Function
1	VCC1	Logic-side Power Supply.
2	GND1	Logic-side Ground pin.
3	RO	Receiver outputs. When REB is low and if (A - B) ≥ -50mV, RO is high; if (A - B) ≤ -200mV, RO is low.
4	REB	Receiver Output Enable. Drive REB low to enable receiver; RO is high impedance when REB is high. Drive REB high and DE low to enter shutdown mode.
5	DE	Transmitter Output Enable. Drive DE high to enable transmitter outputs. The outputs of transmitter are high impedance when DE is low. Drive REB high and DE low to enter shutdown mode.
6	DI	Transmitter Input. With DE high, low state of D forces pin12 (A) to be low and pin13 (B) to be high. Similarly, high state of D forces pin12 (A) to be high and pin13 (B) to be low.
7	GND1	Logic-side Ground pin.
8	GND1	Logic-side Ground pin.
9	GND2	Bus-side Ground pin.
10	GND2	Bus-side Ground pin.
11	nc	No Connection.
12	A	Non-inverting Receiver Input and Non-inverting Transmitter Output
13	B	Inverting Receiver Input and Inverting Transmitter Output
14	nc	No Connection.
15	GND2	Bus-side Ground pin.
16	VCC2	Bus-side Power Supply.

REGULATORY INFORMATION

UL
Certified according to UL 1577 Component Recognition Program
Isolation voltage, 2500 V_{RMS} (1)
File Number: E524663

(1) Production tested ≧ 3000 V_{RMS} for 1 second in accordance with UL 1577

FUNCTIONAL TABLE

Table 1. Transmitter Function Table

TRANSMITTING					
VCC1	VCC2	INPUT (DI)	ENABLE (DE)	OUTPUT (A)	OUTPUT (B)
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	HIGH- Z	HIGH- Z
PU	PU	X	OPEN	HIGH- Z	HIGH- Z
PU	PU	OPEN	H	H	L
PU	PD	X	X	HIGH- Z	HIGH- Z
PD	PD	X	X	HIGH- Z	HIGH- Z

Table 2. Receiver Function Table

RECEIVING				
VCC1	VCC2	DIFFERENTAL INPUT V_{ID} (A – B)	ENABLE (REB)	OUTPUT (RO)
PU	PU	$V_{ID} \geq -0.05$ V	L	H
PU	PU	-0.2V$\leq$ V_{ID} $\leq$-0.05V	L	H/L
PU	PU	$V_{ID} \leq -0.2$ V	L	L
PU	PU	X	H	HIGH- Z
PU	PU	X	OPEN	HIGH- Z
PU	PU	OPEN	L	H
PU	PU	SHORT	L	H
PU	PU	IDLE	L	H
PD	PU	X	X	HIGH- Z

PARAMETER MEASUREMENT INFORMATION

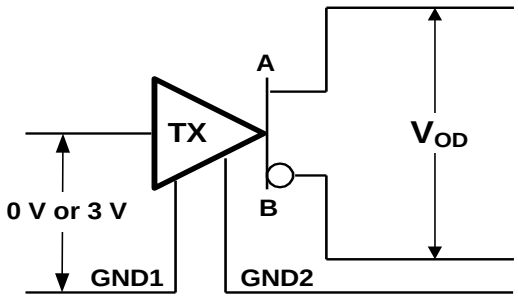


Figure 1. VOD Test Circuit of the transmitter

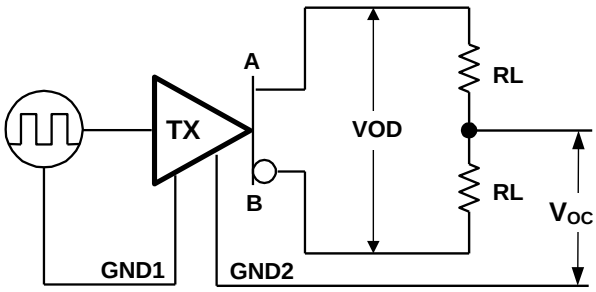
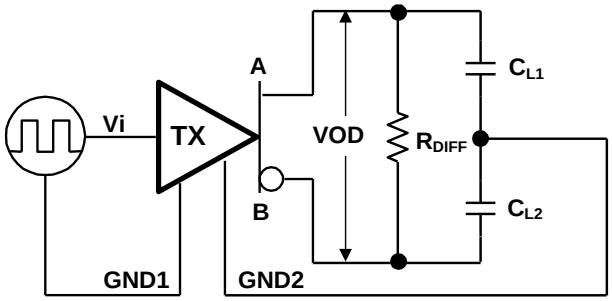


Figure 2. VOD2 and VOC Test circuit of the transmitter



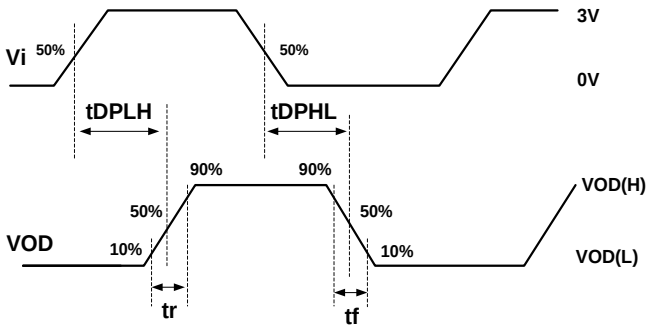
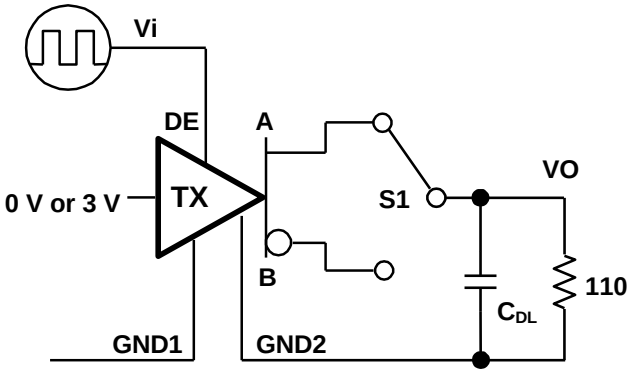


Figure 3. Switching Test Circuit and Voltage Waveforms of the transmitter



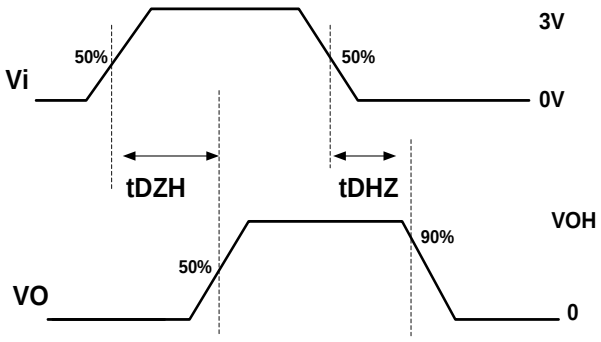


Figure 4. Output Enable and Disable time from High Test Circuit and Voltage Waveforms

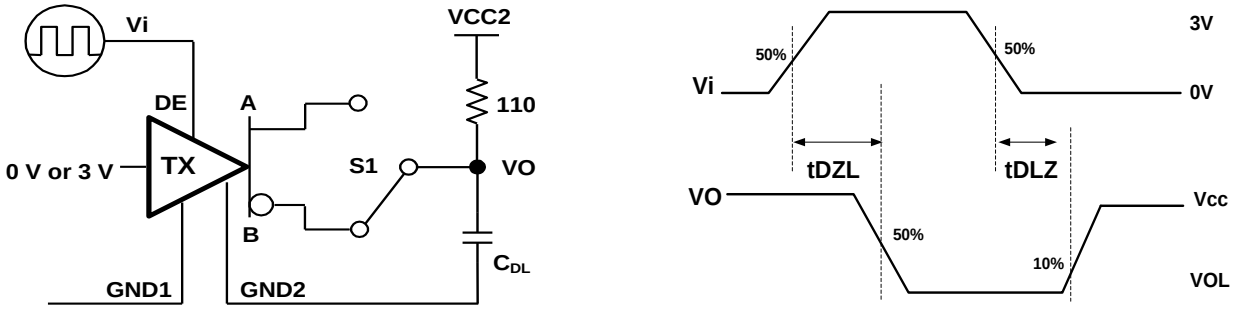


Figure 5. Output Enable and Disable Time from Low Test Circuit and Voltage Waveform

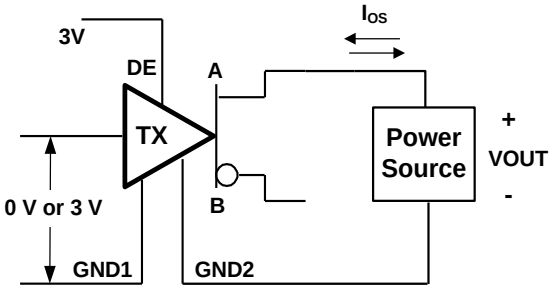


Figure 6. Short-Circuit Output Current of Transmitter.

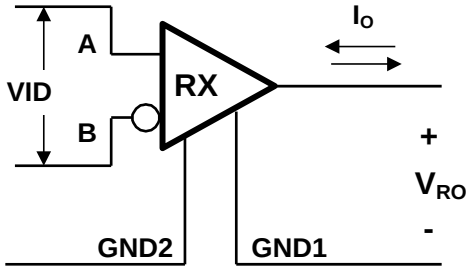
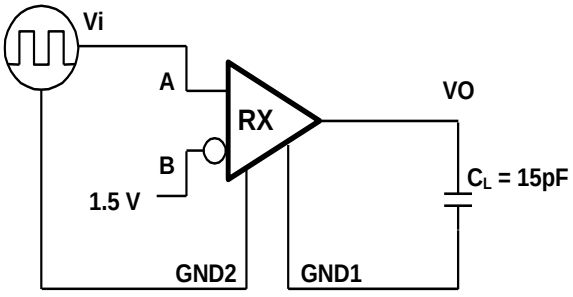


Figure 7. Voltage and Current Definitions of Receiver



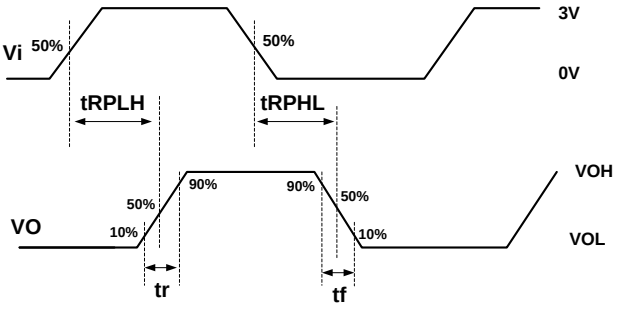
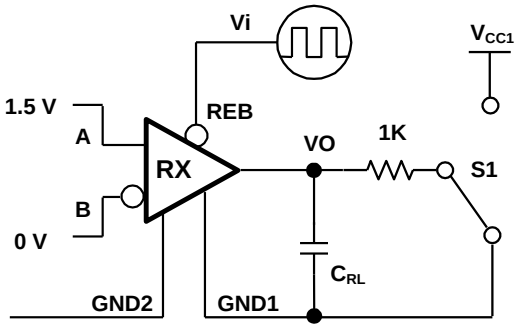


Figure 8. Switching Test Circuit of Receiver



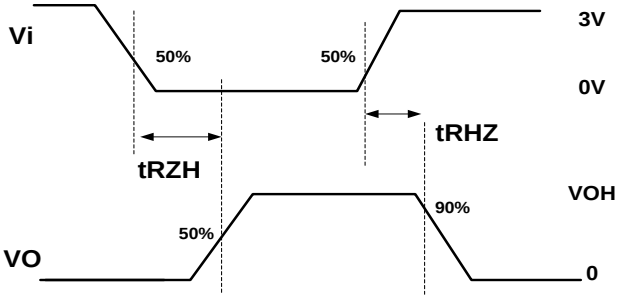


Figure 9. Output High of the Receiver Enable Test Circuit

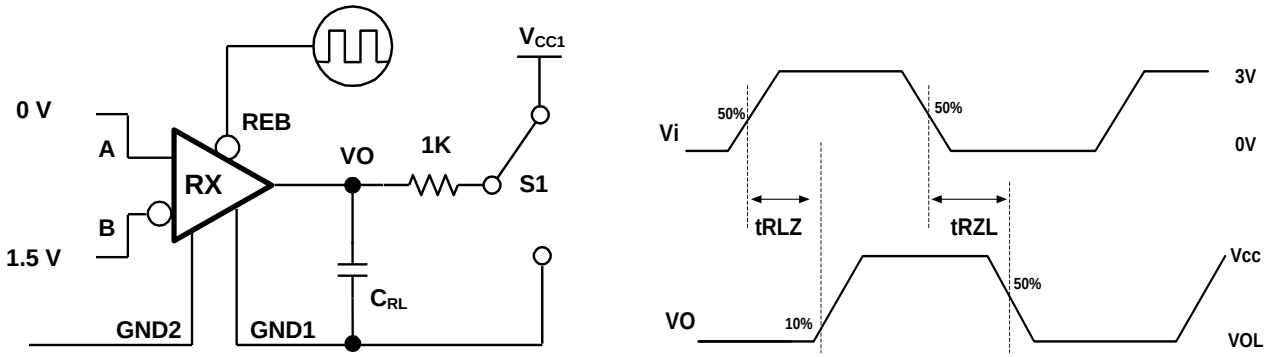


Figure 10. Output Low of the Receiver Enable Test Circuit

Detail Description

The AZRS6412 is a half-duplex isolated RS-485 transceiver IC with IEC61000-4-2 contact ±8kV ESD protection for bus pins (A and B), which contains one transmitter and one receiver inside. This device is fully compliant with the EIA/TIA-485 standard.

The AZRS6412 features the hot-swap glitch free design which guarantees the outputs of the transceiver in a high impedance state during the power-up period until the supply voltage has stabilized. The AZRS6412 with whole chip ESD protected design for all of the I/O pins has robust ESD protection up to both HBM ±8kV and MM ± 600V. Moreover, the latchup immunity of the AZRS6412 is up to ±400mA for all of the pins. For IC self discharge issue, the CDM protection level of the AZRS6412 is up to ±1kV.

Transmitter

The design of the transmitter is a non-inverted translator that converts the single-ended TTL input signal to differential EIA/TIA-485 signal level. The transmitter of the AZRS6412 guarantees 200Kbps data rate communication. When the transmitter is active (DE= HIGH), the single-end TTL input signals of transmitter will be transported to differential output RS485 signals of the transmitter. Under the disable state (DE= LOW), the outputs of transmitter keep at high impedance state. The differential output voltage VA-VB(VOD2) of the AZRS6412 is 2.0V with 54Ω load under Vcc = 5.0V, T= 25°C.

Receiver

The receiver of the AZRS6412 converts the differential EIA/TIA-485 signals to single-end output TTL signal when receiver is in active state (REB=LOW), which incorporates input filtering in addition to input hysteresis. The input filtering enhances the noise immunity under normal operating condition. When the receiver is disable (REB=HIGH), the output of the receiver keeps in high impedance state no matter what the input of the receiver is.

True Fail-Safe

In traditional design, the fail-safe function is implemented by two resistors on the PCB. One resistor is terminated pin A to VCC; the other is terminated pin B to GND to keep RO at high state when bus is idle, which is only the open fail-safe. The AZRS6412 guarantees a receiver output high when the receiver inputs are short, open or idle, that is true fail-safe. The threshold voltage of receiver input is between -50mV and -200mV. If the differential input voltage (A - B) of receiver is greater than or equal to -50mV, receiver output (RO) is logic-high. If (A - B) is less than or equal to -200mV, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage (A - B) is 0V, so the RO is logic-high at that time.

1/8 Unit Load

The RS-485 standard defines both receiver inputs impedance are 12kΩ (1 unit load) and the maximum 32-unit loads on the bus. The AZRS6412 transceiver has a 96kΩ input impedance (1/8 unit load) of the receiver, allowing up to 256 or fewer devices to be connected in parallel on the RS485 bus.

Transmitter Output Protection

The AZRS6412 has the current limitation function and the thermal shutdown protection in the transmitter. Firstly, the function of current limitation provides immediate protection against short circuits over the whole common-mode voltage range (-7V to +12V). Secondly, the function of thermal shutdown protection forces the transmitter outputs into a high impedance state if the die temperature becomes excessive.

LAYOUT GUIDELINES

Figure 11 shows the recommended placement and routing of the decoupling capacitors of the AZRS6412. The recommended distance of decoupling capacitors C1 and C2 on the top layer is less than 5mm from the pins of VCC1 and VCC2. The ground plane layout of GND1 and GND2 is must for the low EMI design

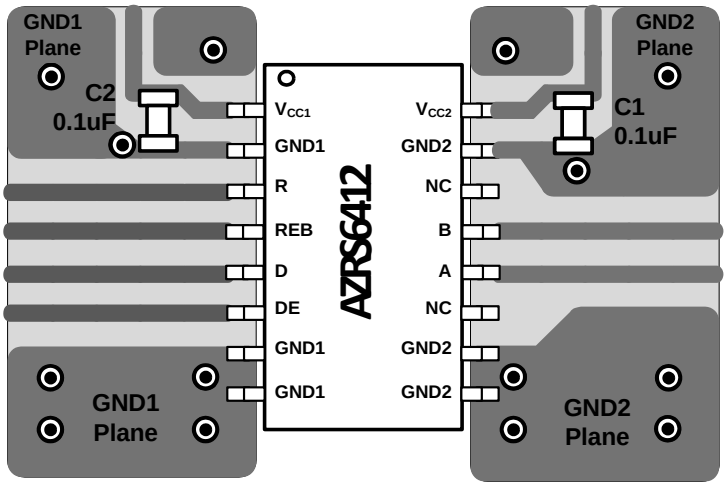
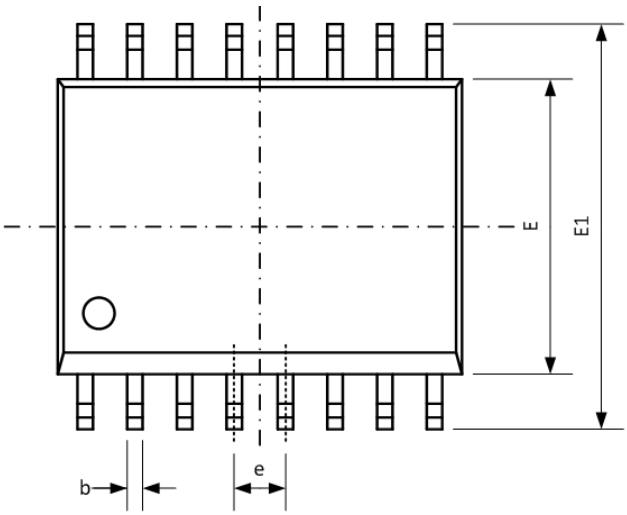


Figure 11. Layout Guideline

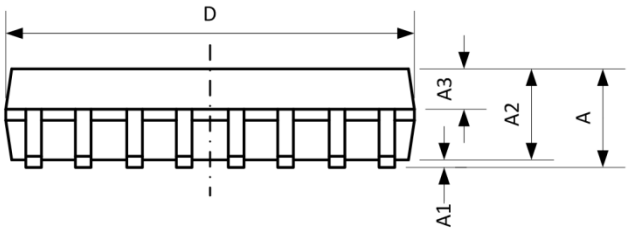
Mechanical Details

WSOIC-16 PACKAGE DIAGRAMS

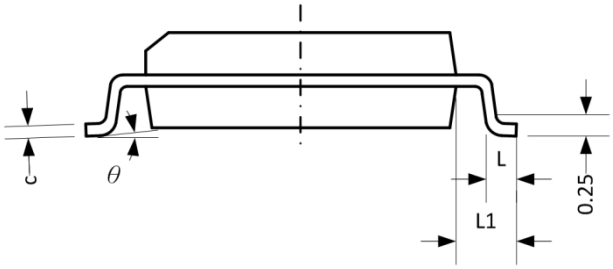
TOP VIEW



SIDE VIEW



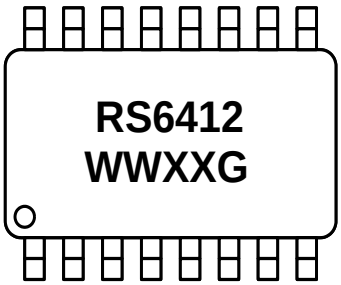
END VIEW



PACKAGE DIMENSIONS

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	-	0.43
c	0.25	-	0.29
D	10.20	10.30	10.40
E1	10.10	10.30	10.50
E	7.40	7.50	7.60
e	1.27 BSC		
L	0.55	-	0.85
L1	1.40 REF		
θ	0^o	-	8^o

MARKING CODE



RS6412 = Device Code
WW = Date Code
XX = Control Code
G = Green Part Indication

Part Number	Marking Code
AZRS6412.RDG	RS6412 WWXXG

Ordering Information

PN#	Material	Type	Reel size	MOQ/internal box	MOQ/carton
AZRS6412.RDG	Green	T/R	13 inch	1 reel=1,500/box	5 boxes=7,500/carton

Revision History

Revision	Modification Description
Revision 2022/08/19	Formal Release